

IN THE CLAIMS:

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

- 1        77. (unchanged) An integrated circuit structure, comprising:
  - 2              a substrate;
  - 3              a field oxide over the substrate, the field oxide having an opening therethrough to a
  - 4              surface of the substrate;
  - 5              a gate electrode over the surface of the substrate and within the opening, the gate
  - 6              electrode having insulating material on a bottom and on two sides of the gate electrode, wherein
  - 7              the insulating material on the bottom of the gate electrode contacts the substrate; and
  - 8              source and drain regions adjacent the insulating material on the gate electrode, each
  - 9              source and drain region including
  - 10              a first portion in the substrate and
  - 11              a second portion on the substrate over the first portion and adjacent to the
  - 12              insulating material on the sides of the gate electrode.

1       78. (unchanged) The integrated circuit structure of claim 77, wherein the opening through the  
2       substrate has substantially vertical sidewalls.

1       79. (unchanged) The integrated circuit structure of claim 78, wherein each source and drain  
2       region is formed between a sidewall of the opening and the insulating material on the sides of  
3       the gate electrode.

1       80. (unchanged) The integrated circuit structure of claim 79, wherein a space between a  
2       sidewall of the opening and the insulating material on the sides of the gate electrode is filled  
3       with material forming the second portion of one of the source and drain regions.

1       81. (unchanged) The integrated circuit structure of claim 77, further comprising:  
2              LDD regions for the source and drain regions formed within the first portion of each  
3              source and drain region.

1       82. (unchanged) The integrated circuit structure of claim 81, wherein the LDD regions are  
2       formed in the substrate beneath the insulating material on the sides of the gate electrode.

1       83. (unchanged) The integrated circuit structure of claim 77, wherein the gate electrode, the  
2       insulating material on the sides of the gate electrode, and the second portions of the source and  
3       drain regions fill the opening.

1       84. (unchanged) The integrated circuit structure of claim 77, an upper surface of the gate  
2       electrode is further from a surface of the substrate than an upper surface of the field oxide.

1       85. (twice amended) The integrated circuit structure of claim 77, wherein the first and second  
2       portions of the source and drain regions are both formed of a semiconductor material doped to  
3       include lightly doped regions within at least the first portions and heavily doped regions within  
4       at least the second portions.

1       86. (unchanged) The integrated circuit structure of claim 77, wherein the second portions of the  
2       source and drain regions each form contact regions for source/drain contacts.

1       87. (unchanged) The integrated circuit structure of claim 82, wherein the LDD regions are the  
2       first portions of the source and drain regions.

1       88. (unchanged) The integrated circuit structure of claim 77, wherein the second portions of the  
2       source and drain regions have a dopant concentration suitable for heavily doped source/drain  
3       regions.

1       89. (unchanged) The integrated circuit structure of claim 88, wherein the dopant concentration  
2       within the second portions of the source and drain regions is formed by implanting dopants at  
3       a dosage of approximately  $6 \times 10^{15}$  at 40 KeV.

1       90. (unchanged) The integrated circuit structure of claim 88, wherein the LDD regions are the  
2       first portions of the source and drain regions.

1       91. (unchanged) The integrated circuit structure of claim 88, wherein the first portions of the  
2       source and drain regions include the LDD regions and portions of heavily doped source and  
3       drain regions.

1       92. (unchanged) The integrated circuit structure of claim 77, further comprising:  
2              a refractory metal silicide on the second portions of the source and drain regions include  
3              the LDD regions and portions of heavily doped source and drain regions.

1        93. (unchanged) An integrated circuit structure, comprising:

2              a field oxide over a substrate, the field oxide having an opening therethrough to a surface

3              of the substrate;

4              a gate structure on the surface of the substrate within the opening, the gate structure

5              having insulating material on a bottom and sides of the gate electrode;

6              doped regions within portions of the substrate within the opening which are adjacent to

7              and extend beneath the gate structure, wherein the doped regions within the substrate are at least

8              lightly doped; and

9              doped semiconductor material on the substrate within the opening adjacent to the gate

10             structure and over each of the doped regions within the substrate, the doped semiconductor

11             material doped to a concentration suitable for heavily doped source and drain regions,

12             wherein the doped regions within the substrate and doped semiconductor material form

13             a source and a drain for a transistor including the gate structure.

1        94. (unchanged) The integrated circuit structure of claim 93, wherein the doped semiconductor

2             material on the substrate has a dopant concentration formed by implanting dopants at a dosage

3             of approximately  $6 \times 10^{15}$  at 40 KeV.

1       95. (unchanged) The integrated circuit structure of claim 93, wherein an upper surface of the  
2       doped semiconductor material is coated with a refractory metal silicide to form a contact region  
3       to the source and drain.

1       96. (unchanged) A transistor, comprising:  
2              a gate electrode on an insulating layer over a substrate surface;  
3              insulating sidewall layers on the gate electrode; and  
4              doped source and drain regions within portions of the substrate adjacent to and extending  
5       beneath the insulating sidewall layers and within semiconductor material on the substrate  
6       adjacent to the insulating sidewall layers,  
7              wherein the portions of the source and drain regions within the substrate are at least  
8       lightly doped and the portions of the source and drain regions within the semiconductor material  
9       on the substrate are doped to a concentration suitable for heavily doped source and drain  
10      regions.